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BAKER BOTTS L.L.P.
2001 ROSS AVENUE
SUITE 600
DALLAS, TX 75201-2980

EXAMINER	
MOORE JR, MICHAEL J	
ART UNIT	PAPER NUMBER
2419	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptomail1@bakerbotts.com
glenda.orrantia@bakerbotts.com

Office Action Summary	Application No.	Applicant(s)	
	10/025,599	MARSHALL ET AL.	
	Examiner	Art Unit	
	MICHAEL J. MOORE, JR.	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-16 and 45-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-16 and 45-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to the rejections of *amended* claim(s) **1-4, 7-16, and 45-66** under 35 U.S.C. 103(a) in view of *Muntz (U.S. 6,532,215)* have been fully considered and are persuasive. Therefore, these particular rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of *Gammel et al. (U.S. 5,974,363)* as provided below.

Claim Objections

2. Claims **46 and 67-72** are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Specifically, it appears that claim **46** does not further limit now *amended* claim **45**. Similarly, new claims **67-72** do not appear to further limit *amended* claims **1, 45, 60, 65, and 66** or previously presented claim **55**.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims **50 and 52** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim **50** recites the limitation "the termination circuit" in line 2. There is insufficient antecedent basis for this limitation in the claim.

6. Claim **52** recites the limitation "the termination circuit" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims **45-54 and 68** are rejected under 35 U.S.C. 102(b) as being anticipated by Gammel et al. (U.S. 5,974,363) (hereinafter "Gammel"). *Gammel* teaches all of the limitations of the specified claims with the reasoning that follows.

Regarding claims **45, 46, and 68**, "a method for self-testing a portion of a line card having a transmit channel and a receive channel coupled to a combined transmit and receive channel and also having a digital signal processor for manipulating data received by the line card" is anticipated by the self-testing of line card shown in Figure 2 having a digital signal processor and having a transmit path (channel) as well as a receive path (channel) both having amplifiers (within element 7536), which paths are coupled to a SLIC (combined channel) as shown in Figure 2.

"Transmitting a test signal through at least a portion of the transmit channel toward the combined channel" is anticipated by the tone generator of the digital signal processor produces a tone signal (test signal) for transmission toward and testing of the

tip and ring lines (toward SLIC combined channel) as spoken of on column 7, line 58-65.

Lastly, "determining whether any components in the transmit channel or receive channel are malfunctioning by detecting, by the digital signal processor, any resulting signal in the receive channel and introducing a reflection in the combined channel" is anticipated by the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

Regarding claim **47**, "comparing the detected signal to an expected detected signal" is anticipated by the comparison of test routine results (detected signals) with predefined test limits (expected signals) as spoken of on column 11, lines 1-3.

Regarding claim **48**, "filtering the test signal within the portion of the transmit channel" is anticipated by the filtering in the transmit and receive paths as shown in Figure 1.

Regarding claim **49**, "comparing the detected signal to the filtered test signal" is anticipated by the filtering in the transmit and receive paths as shown in Figure 1 as well as the comparison of test routine results (detected signals) with predefined test limits (expected signals) as spoken of on column 11, lines 1-3.

Regarding claim **50**, "wherein the impedance of the termination circuit is approximately the characteristic impedance of an input line to the line card" is anticipated by the use of terminating resistance in forward loop testing as spoken of on column 6, lines 30-37.

Regarding claim **51**, "introducing an open in the combined channel" is anticipated by the open circuit test spoken of on column 7, lines 58-62.

Regarding claim **52**, "providing a switch in the combined channel before the termination circuit" is anticipated by switches sw2 and sw4 within the SLIC (combined channel) as shown in Figure 2.

Regarding claim **53**, "selectively opening or closing the switch to test the one or more of the components" is anticipated by the use of switches sw2 and sw4 in the open circuit test spoken of on column 7, line 58 – column 8, line 5.

Regarding claim **54**, "shorting the combined channel to itself" is anticipated by the open circuit test spoken of on column 7, line 58 – column 8, line 5.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims **1, 2, 4, and 7-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gammel et al. (U.S. 5,974,363) (hereinafter "Gammel") in view of McMillian et al. (U.S. 6,229,814) (hereinafter "McMillian") and in further view of Li (U.S. 2002/0118819).

Regarding claim **1**, *Gammel* teaches a line card in Figure 2 having a digital signal processor as shown.

Gammel also teaches the line card having a transmit path (channel) as well as a receive path (channel) both having amplifiers (within element 7536), which paths are coupled to a SLIC (combined channel) as shown in Figure 2.

Gammel also teaches an AC interface and current sensor elements (electrical components) within the SLIC (combined channel) as shown in Figure 2.

Gammel also teaches switches sw2 and sw4 within the SLIC (combined channel) as shown in Figure 2.

Gammel also teaches where the tone generator of the digital signal processor produces a tone signal (test signal) for transmission toward and testing of the tip and ring lines (toward SLIC combined channel) as spoken of on column 7, line 58-65.

Gammel also teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

While *Gammel* also teaches the use of terminating resistance in forward loop testing as spoken of on column 6, lines 30-37, *Gammel* does not explicitly teach "terminating the combined channel with a termination network, the termination network having a desired impedance".

However, *McMillian* teaches a system in Figure 3 used for DSL line testing, where tip and ring leads of a test bus 80 (combined channel) are coupled to link impedance simulation circuits 71 and 75 (termination network) comprising resistor-capacitor networks that are controllably configured to provide a prescribed test bus termination impedance as spoken of on column 4, line 59 – column 5, line 4.

These references are considered to be analogous art in that they are both concerned with the use of test signaling to detect fault conditions in a network environment.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the termination network teachings of *McMillian* to the above teachings of *Gammel* in order to provide effective testing of the tip and ring portions of the line while spoofing the presence of a network or customer interface, thereby reducing the amount of overhead sent over the data network.

While *McMillian* teaches that the above termination network may be configured to provide particular test bus impedance, *McMillian* does not explicitly teach where the desired impedance is approximately equal to a characteristic impedance of a communication line conventionally used with the line card, and where this characteristic impedance is 100 ohms.

However, *Li* teaches where the impedance of a subscriber line in the xDSL band is known to fall in the range of 100-135 ohms as spoken of on page 3, paragraph 31.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to combine the impedance teachings of *Li* with the teachings of *Gammel* in view of *McMillian* to provide a termination circuit having matched impedance that provides accurate testing of a DSL system.

Regarding claim **2**, *Gammel* further teaches the receive path and transmit path coupled to the SLIC (combined channel) via an AC interface (hybrid) as shown in Figure 2.

Regarding claim **4**, *Gammel* further teaches the receive path and transmit path coupled to the SLIC (combined channel) via an AC interface (connector) as shown in Figure 2.

Regarding claim **7**, *Gammel* further teaches where the tone generator of the digital signal processor produces a tone signal (test signal) for transmission toward and testing of the tip and ring lines (toward SLIC combined channel) as spoken of on column 7, line 58-65.

Regarding claims **8-10**, *Gammel* further teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch (component) is faulty as spoken of on column 7, line 65 – column 8, line 5.

Regarding claims **11 and 12**, *Gammel* further teaches the filtering in the transmit and receive paths as shown in Figure 1.

Regarding claim **13**, *Gammel* further teaches switches sw2 and sw4 within the SLIC (combined channel) as shown in Figure 2, as well as the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

Regarding claim **14**, *Gammel* further teaches the comparison of test routine results (detected signals) with predefined test limits (expected signals) as spoken of on column 11, lines 1-3.

Regarding claim **15**, *Gammel* does not teach a termination network formed on the line card.

However, *McMillian* teaches the link impedance simulation circuits 71 and 75 (termination network) of the multi-circuit line card shown in Figure 3.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the termination network teachings of *McMillian* to the above teachings of *Gammel* in order to provide effective testing of the tip and ring portions of the DSL line while spoofing the presence of a network or customer interface, thereby reducing the amount of overhead sent over the data network.

Regarding claim **16**, *Gammel* does not teach a termination network formed external to the line card.

However, *McMillian* teaches the link impedance simulation circuits 71 and 75 (termination network) of the multi-circuit line card shown in Figure 3.

McMillian does not explicitly teach where the termination network is external to the line card.

However, it would have been obvious to someone of ordinary skill in the art, given the teachings of *McMillian*, to have the termination circuit external rather than internal to the system in order to make the termination network modular in design for use with testing multiple line cards.

12. Claims **55-62, 64-67, and 69-72** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gammel et al. (U.S. 5,974,363) (hereinafter "Gammel") in view of McMillian et al. (U.S. 6,229,814) (hereinafter "McMillian").

Regarding claim **55**, *Gammel* teaches a line card in Figure 2 having a digital signal processor as shown.

Gammel also teaches the line card having a transmit path (channel) as well as a receive path (channel) both having amplifiers (within element 7536), which paths are coupled to a SLIC (combined channel) as shown in Figure 2.

Gammel also teaches switches sw2 and sw4 within the SLIC (combined channel) as shown in Figure 2 used for testing as spoken of on column 7, lines 58-62.

Gammel also teaches where the tone generator of the digital signal processor produces a tone signal (test signal) for transmission toward and testing of the tip and ring lines (toward SLIC combined channel) as spoken of on column 7, line 58-65.

Gammel also teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

Gammel further teaches the filtering in the transmit and receive paths as shown in Figure 1.

While *Gammel* also teaches the use of terminating resistance in forward loop testing as spoken of on column 6, lines 30-37, *Gammel* does not explicitly teach "terminating the combined channel with a termination circuit, the termination circuit having an impedance and comprising one or more resistors and one or more capacitors".

However, *McMillian* teaches a system in Figure 3 used for DSL line testing, where tip and ring leads of a test bus 80 (combined channel) are coupled to link impedance simulation circuits 71 and 75 (termination network) comprising resistor-capacitor networks that are controllably configured to provide a prescribed test bus termination impedance as spoken of on column 4, line 59 – column 5, line 4.

These references are considered to be analogous art in that they are both concerned with the use of test signaling to detect fault conditions in a network environment.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the termination network teachings of *McMillian* to the above teachings of *Gammel* in order to provide effective testing of the

tip and ring portions of the line while spoofing the presence of a network or customer interface, thereby reducing the amount of overhead sent over the data network.

Regarding claim **56**, *Gammel* further teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

Regarding claim **57**, *Gammel* further teaches the filtering in the transmit and receive paths through filter components as shown in Figure 1.

Regarding claims **58 and 59**, *Gammel* further teaches the comparison of test routine results (detected signals) with predefined test limits (expected signals) as spoken of on column 11, lines 1-3.

Regarding claim **60**, *Gammel* teaches a line card in Figure 2 having a digital signal processor as shown.

Gammel also teaches the line card having a transmit path (channel) as well as a receive path (channel) both having amplifiers (within element 7536), which paths are coupled to a SLIC (combined channel) as shown in Figure 2.

Gammel also teaches switches sw2 and sw4 within the SLIC (combined channel) as shown in Figure 2 used for testing as spoken of on column 7, lines 58-62.

Gammel also teaches where the tone generator of the digital signal processor produces a tone signal (test signal) for transmission toward and testing of the tip and ring lines (toward SLIC combined channel) as spoken of on column 7, line 58-65.

Gammel also teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

Gammel further teaches the filtering in the transmit and receive paths as shown in Figure 1.

While *Gammel* also teaches the use of terminating resistance in forward loop testing as spoken of on column 6, lines 30-37, *Gammel* does not explicitly teach "a termination circuit operable to terminate the combined channel".

However, *McMillian* teaches a system in Figure 3 used for DSL line testing, where tip and ring leads of a test bus 80 (combined channel) are coupled to link impedance simulation circuits 71 and 75 (termination network) comprising resistor-capacitor networks that are controllably configured to provide a prescribed test bus termination impedance as spoken of on column 4, line 59 – column 5, line 4.

These references are considered to be analogous art in that they are both concerned with the use of test signaling to detect fault conditions in a network environment.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the termination network teachings of *McMillian* to the above teachings of *Gammel* in order to provide effective testing of the tip and ring portions of the line while spoofing the presence of a network or customer interface, thereby reducing the amount of overhead sent over the data network.

Regarding claim **61**, *Gammel* further teaches the use of terminating resistance in forward loop testing as spoken of on column 6, lines 30-37.

Regarding claim **62**, *Gammel* further teaches an AC interface and current sensor elements (electrical components) within the SLIC (combined channel) as shown in Figure 2.

Regarding claim **64**, *Gammel* further teaches the receive path and transmit path coupled to the SLIC (combined channel) via an AC interface (hybrid) as shown in Figure 2.

Regarding claim **65**, *Gammel* teaches a line card in Figure 2 having a digital signal processor as shown.

Gammel also teaches the line card having a transmit path (channel) as well as a receive path (channel) both having amplifiers (within element 7536), which paths are coupled to a SLIC (combined channel) as shown in Figure 2.

Gammel also teaches switches sw2 and sw4 within the SLIC (combined channel) as shown in Figure 2 used for testing as spoken of on column 7, lines 58-62.

Gammel also teaches where the tone generator of the digital signal processor produces a tone signal (test signal) for transmission toward and testing of the tip and ring lines (toward SLIC combined channel) as spoken of on column 7, line 58-65.

Gammel also teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

Gammel further teaches the filtering in the transmit and receive paths as shown in Figure 1.

While *Gammel* also teaches the use of terminating resistance in forward loop testing as spoken of on column 6, lines 30-37, *Gammel* does not explicitly teach "terminating the combined channel with a termination circuit, the termination circuit having an impedance and comprising one or more resistors and one or more capacitors".

However, *McMillian* teaches a system in Figure 3 used for DSL line testing, where tip and ring leads of a test bus 80 (combined channel) are coupled to link impedance simulation circuits 71 and 75 (termination network) comprising resistor-capacitor networks that are controllably configured to provide a prescribed test bus termination impedance as spoken of on column 4, line 59 – column 5, line 4.

These references are considered to be analogous art in that they are both concerned with the use of test signaling to detect fault conditions in a network environment.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the termination network teachings of *McMillian* to the above teachings of *Gammel* in order to provide effective testing of the tip and ring portions of the line while spoofing the presence of a network or customer interface, thereby reducing the amount of overhead sent over the data network.

Regarding claim **66**, *Gammel* teaches a line card in Figure 2 having a digital signal processor as shown.

Gammel also teaches the line card having a transmit path (channel) as well as a receive path (channel) both having amplifiers (within element 7536), which paths are coupled to a SLIC (combined channel) as shown in Figure 2.

Gammel also teaches switches sw2 and sw4 within the SLIC (combined channel) as shown in Figure 2 used for testing as spoken of on column 7, lines 58-62.

Gammel also teaches where the tone generator of the digital signal processor produces a tone signal (test signal) for transmission toward and testing of the tip and ring lines (toward SLIC combined channel) as spoken of on column 7, line 58-65.

Gammel also teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

Gammel further teaches the filtering in the transmit and receive paths as shown in Figure 1.

While *Gammel* also teaches the use of terminating resistance in forward loop testing as spoken of on column 6, lines 30-37, *Gammel* does not explicitly teach "a termination circuit operable to terminate the combined channel".

However, *McMillian* teaches a system in Figure 3 used for DSL line testing, where tip and ring leads of a test bus 80 (combined channel) are coupled to link impedance simulation circuits 71 and 75 (termination network) comprising resistor-capacitor networks that are controllably configured to provide a prescribed test bus termination impedance as spoken of on column 4, line 59 – column 5, line 4.

These references are considered to be analogous art in that they are both concerned with the use of test signaling to detect fault conditions in a network environment.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to apply the termination network teachings of *McMillian* to the above teachings of *Gammel* in order to provide effective testing of the tip and ring portions of the line while spoofing the presence of a network or customer interface, thereby reducing the amount of overhead sent over the data network.

Regarding claims **67 and 69-72**, *Gammel* further teaches the detection of reflected signals (resulting signal) by the digital signal processor in order to detect whether a particular switch is faulty (malfunctioning) as spoken of on column 7, line 65 – column 8, line 5.

13. Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gammel et al. (U.S. 5,974,363) (hereinafter "Gammel") in view of McMillian et al. (U.S. 6,229,814) (hereinafter "McMillian") in view of Li (U.S. 2002/0118819) and in further view of Itri (U.S. 6,909,781).

Regarding claim **3**, *Gammel* in view of *McMillian* in view of *Li* teaches the limitations described above.

Gammel in view of *McMillian* in view of *Li* does not teach where the one or more electrical components in the combined channel comprise a transformer.

However, *Itri* teaches a DSL line testing system in Figure 8 containing a scaling transformer coupled to hybrid 218.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to use a scaling transformer as in *Itri* in the system of *Gammel* in view of *McMillian* in view of *Li* in order to provide a way to adjust the voltage of incoming and outgoing signals to an appropriate level.

14. Claim **63** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gammel et al. (U.S. 5,974,363) (hereinafter "Gammel") in view of McMillian et al. (U.S. 6,229,814) (hereinafter "McMillian") and in further view of Itri (U.S. 6,909,781).

Regarding claim **63**, *Gammel* in view of *McMillian* teaches the limitations described above.

Gammel in view of *McMillian* does not teach where the one or more electrical components in the combined channel comprise a transformer.

However, *Itri* teaches a DSL line testing system in Figure 8 containing a scaling transformer coupled to hybrid 218.

At the time of the invention, it would have been obvious to someone of ordinary skill in the art, given these references, to use a scaling transformer as in *Itri* in the system of *Gammel* in view of *McMillian* in order to provide a way to adjust the voltage of incoming and outgoing signals to an appropriate level.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bliven et al. (U.S. 5,111,497) is another reference considered pertinent to this application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL J. MOORE, JR., whose telephone number is (571)272-3168. The examiner can normally be reached on Monday-Friday (7:30am - 4:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayanti K. Patel can be reached at (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J. Moore, Jr./
Examiner, Art Unit 2419